IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re. U	U.S. Patent Application of)				-
HASE	GGAWA et al.)				
Applio	(ation Number: 10/058,787)	Unit 2813			
Filed:))	Examiner Dolan, Jenni	fer M		
For:	SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE, METHOD OF TESTING SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND METHOD OF MANUFACTURING SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE		* * * * * * * * * * * * * * * * * * *	TECH		
Аттоі	RNEY DOCKET NO. ASAM.0038		÷	HOLOG	SEP 29	ACE OF
for Pat	able Assistant Commissioner tents ngton, D.C. 20231			ECHNOLOGY CENTER 28	2003	RECEIVED
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[x] The fee for submission of additional claims is calculated as shown below:

Sir:

For	TOTAL WITH NEW CLAIMS ADDED	TOTAL CURRENTLY ON FILE	CLAIMS PAID	RATE	CALCULATION
Total Claims	12	12	(Over 20)	x \$18	0
Independent Claims	3	3	(Over 3)	x \$84	0
MULTIPLE DEPENDENT CLAIM(S)				+ \$280	0
	LING BY SMALL ENTITY UFIED STATEMENT MUS	(note 37 C.F.R. §§ 1.9, 1.27 T BE ATTACHED	, 1.28).	x ½	
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In addit	ion	, the below-identified communications are submitted	ed i	n the above-captioned application or proceeding:
		[x] Response to Office Action	[] Petition for Extension of Time (month)
		(with Claim Amendments)	[] Terminal Disclaimer
		[] Substitute Specification & marked-up copy	[] Letter to Draftsperson w/ sheets of drawings

 ,		Assignment Petition under	
[]	Please charge my Deposit Account Number in the A duplicate copy of this paper is enclosed.	e amount of to cover the fees for _ osed.	
[]] A check in the amount of \$ to cover the fee is enclosed.		
[x] The Commissioner is hereby authorized to charge any additional fees associated with this commincluding patent application filing fees and processing fees under 37 C.F.R. § 1.16 and 1.17, or overpayment to Deposit Account Number 08-1480 .			
	Respectfully sub	mitted,	
	Stanley P. Fisher		
	Registration Num Juan Carlos A A Registration No.	All Jarquez	
	/	_	

REED SMITH LLP

3110 Fairview Park Drive Suite 1400 Falls Church, Virginia 22042 (703) 641-4200 September 25, 2003

- 1 -#1/a 10/1/3 Surles IN THE UNITED STATES PATENT AND TRADEMARK OFFIC In re U.S. Patent Application of HASEGAWA et al. **Unit 2813** Application Number: 10/058,787 **Examiner** Filed: January 30, 2002 Dolan, Jennifer M SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE, METHOD OF TESTING SEMICONDUCTOR

ATTORNEY DOCKET NO. ASAM.0038

CIRCUIT DEVICE

INTEGRATED CIRCUIT DEVICE AND METHOD OF MANUFACTURING SEMICONDUCTOR INTEGRATED)

Honorable Assistant Commissioner for Patents Washington, D.C. 20231

RESPONSE AND AMENDMENT UNDER 37 C.F.R. §1.111

Sir:

For:

This is in response to the Office Action dated September 9, 2003, the period for response to which will expire on October 9, 2003. Applicants hereby timely elect the continuing prosecution of Claims 1-8, without traverse.